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1 Introduction

The iGPIB 72120 provides an interface between the PCI bus system and the GPIB specified in the IEEE Std. 488.1-1987 and 488.2-1987. The design is fully synchronous which provides for enhanced reliability compared to asynchronous ASIC designs. The iGPIB 72120 is used with low-cost external drivers that implement the interface to the GPIB bus lines.

The 72120 is register compatible with the NEC μ PD 7210 C in GPIB Talker/Listener applications. GPIB Controller functions has been removed from the design.

- Pb-free meeting the RoHS Directive (2002/95/EC)
- PCI v2.2 32-bit/33MHz Target with 3.3 VCC, 3.3/5.0 VIO
- 0.35 μ m four-layer metal CMOS process
- The following IEEE488.1 interface function are provided:
 - Source Handshake (SH1)
 - Acceptor Handshake (AH1)
 - Talker or Extended Talker (T5 or TE5)
 - Listener or Extended Listener (L3 or LE3)
 - Service Request (SR1)
 - Remote/Local (RL1)
 - Parallel Poll: remote configuration(PP1), local configuration (PP2)
 - Device Clear (DC1)
 - Device Trigger (DT1)
 - No Controller capability (C0)
- Meets all requirements of IEEE488.2-1987:
 - Bus line monitoring
 - Preferred request service implementation
 - Does not source any data without Listeners
 - Listener function disable

2 Signal Descriptions

The iGPIB 72120 is available in a 144-pin TQFP package. The physical pin types are listed in the following table:

Pin Type Nomenclature

Prefix	Description
I	Input
IO	Input/Output
O	Output
zO	Output with Disable
VCC	VCC pin
VCCIO	VCCIO pin
GND	GND pin
NU	Not used

Logical signals are assigned to physical pins. Their names follow a common nomenclature in which signal functions are prefixed by their wide and direction:

Signal Type Nomenclature

Prefix	Description
iob*	I/O bit
iow* [0:3]	I/O vector with width specification
ob*	Output bit
ow* [0:3]	Output vector with width specification
ib*	Input bit
iw* [0:3]	Output vector with width specification
pci*	Signals defined by the PCI specification
CAPS	Special purpose signals start with capital letters

The following table lists all the external signals in order of their pin assignment.

Signals Listed by Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal
1	obNDACoEn	2	obNRFDoeN	3	obREN
4	PCI_RSTN	5	NU (Do not connect)	6	obSRQoeN
7	VCC	8	ibATN	9	ibDAV
10	ibEOI	11	ibIFC	12	ibSRQ
13	ibREN	14	ibNRFD	15	GND
16	ibNDAC	17	NU (Connect to Gnd)	18	NU (Connect to Gnd)



Pin	Signal	Pin	Signal	Pin	Signal
19	VCC	20	RSTN	21	CLK
22	VCC	23	pciINTA	24	pciAD[31]
25	pciAD[30]	26	pciAD[29]	27	pciAD[28]
28	pciAD[27]	29	pciAD[26]	30	GND
31	pciAD[25]	32	pciAD[24]	33	pciCBEN[3]
34	pciIDSEL	35	pciAD[23]	36	pciAD[22]
37	pciAD[21]	38	JTAG: TDI (Connect to VCC)	39	pciAD[20]
40	pciAD[19]	41	pciAD[18]	42	VCC
43	pciAD[17]	44	pciAD[16]	45	pciCBEN[2]
46	pciFRAMEN	47	pciIRDYN	48	pciTRDYN
49	pciDEVSELN	50	GND	51	pciSTOPN
52	pciPERRN	53	pciSERRN	54	GND
55	pciPAR	56	pciCBEN[1]	57	pciAD[15]
58	VCCIO	59	pciAD[14]	60	pciAD[13]
61	pciAD[12]	62	pciAD[11]	63	pciAD[10]
64	pciAD[9]	65	pciAD[8]	66	GND
67	pciCBEN[0]	68	pciAD[7]	69	pciAD[6]
70	pciAD[5]	71	JTAG: TRSTB (Connect to GND)	72	JTAG: TMS (Connect to VCC)
73	pciAD[4]	74	pciAD[3]	75	pciAD[2]
76	pciAD[1]	77	pciAD[0]	78	NU (Connect to Gnd)
79	VCC	80	NU (Do not connect)	81	NU (Connect to Gnd)
82	NU (Do not connect)	83	NU (Do not connect)	84	NU (Do not connect)
85	NU (Do not connect)	86	NU (Do not connect)	87	GND
88	NU (Do not connect)	89	NU (Connect to Gnd)	90	NU (Connect to Gnd)
91	VCC	92	NU (Connect to Gnd)	93	NU (Connect to Gnd)
94	VCC	95	NU (Do not connect)	96	NU (Do not connect)
97	NU (Do not connect)	98	NU (Do not connect)	99	NU (Do not connect)
100	NU (Connect to Gnd)	101	NU (Connect to Gnd)	102	GND
103	obTRG	104	iwDIO[1]	105	iwDIO[2]
106	iwDIO[3]	107	iwDIO[4]	108	iwDIO[5]
109	JTAG: TCK (Connect to GND)	110	STM(Connect to GND)	111	iwDIO[6]
112	iwDIO[7]	113	iwDIO[8]	114	VCC
115	owDIO[1]	116	owDIOoen[1]	117	owDIO[2]
118	owDIOoen[2]	119	owDIO[3]	120	owDIOoen[3]
121	owDIO[4]	122	GND	123	owDIOoen[4]
124	owDIO[5]	125	owDIOoen[5]	126	GND

Pin	Signal	Pin	Signal	Pin	Signal
127	owDIO[6]	128	owDIOoen[6]	129	owDIO[7]
130	VCCIO	131	owDIOoen[7]	132	owDIO[8]
133	owDIOoen[8]	134	obATN	135	obATNoen
136	obDAV	137	obDAVoен	138	GND
139	obEOI	140	obEOloen	141	obIFC
142	obIFC_RENoen	143	JTAG: TDO (Floating)	144	NU (Do not connect)

Signal Functional Description

Signal	Type	Pin	Description
ibATN	I	8	GPIB input lines. To be connected to SN74LVC244ADBR transceiver outputs for each GPIB line.
ibDAV	I	9	
ibEOI	I	10	
ibIFC	I	11	
ibNDAC	I	16	
ibNRFD	I	14	
ibREN	I	13	
ibSRQ	I	12	
iwDIO[1]	I	104	
iwDIO[2]	I	105	
iwDIO[3]	I	106	
iwDIO[4]	I	107	
iwDIO[5]	I	108	
iwDIO[6]	I	111	
iwDIO[7]	I	112	
iwDIO[8]	I	113	
obATNoen	O	135	GPIB output enable control lines. To be connected to SN74LVTH125DBR transceiver output enable inputs. Define the GPIB line levels. Output transceivers for ATN, IFC, REN are not required in talker/listener applications.
obIFC_RENoen	O	142	
obNDACoen	O	1	
obDAVoен	O	137	
obEOloen	O	140	
obNRFDoen	O	2	
obSRQoen	O	6	
owDIOoen[1]	O	116	
owDIOoen[2]	O	118	
owDIOoen[3]	O	120	
owDIOoen[4]	O	123	

Signal	Type	Pin	Description
owDIOoen[5]	O	125	<p>GPIB output data lines. To be connected to SN74LVTH125DBR transceiver data inputs. Define the GPIB line level if the corresponding transceiver is enabled. The inputs of the SRQ, NDAC, NRFD line transceivers must be tied to GND. Output transceivers for ATN, IFC, REN are not required in talker/listener applications.</p>
owDIOoen[6]	O	128	
owDIOoen[7]	O	131	
owDIOoen[8]	O	133	
obATN	O	134	
obIFC	O	141	
obREN	O	3	
obDAV	O	136	
obEOI	O	139	
owDIO[1]	O	115	
owDIO[2]	O	117	
owDIO[3]	O	119	
owDIO[4]	O	121	
owDIO[5]	O	124	
owDIO[6]	O	127	
owDIO[7]	O	129	
owDIO[8]	O	132	
CLK	I	21	PCI Clk 33 MHz
PCI_RSTN	I	4	PCI RSTN
RSTN	I	20	
pciCBEN[0]	I	67	PCI control signals
pciCBEN[1]	I	56	
pciCBEN[2]	I	45	
pciCBEN[3]	I	33	
pciFRAMEN	I	46	
pciIDSEL	I	34	
pciIRDYN	I	47	
pciDEVSELN	IO	49	
pciPAR	IO	55	
pciPERRN	IO	52	
pciSERRN	IO	53	
pciSTOPN	IO	51	
pciTRDYN	IO	48	
pciINTA	O	23	
pciAD[0]	IO	77	PCI address/data signals
pciAD[1]	IO	76	

Signal	Type	Pin	Description
pciAD[2]	IO	75	
pciAD[3]	IO	74	
pciAD[4]	IO	73	
pciAD[5]	IO	70	
pciAD[6]	IO	69	
pciAD[7]	IO	68	
pciAD[8]	IO	65	
pciAD[9]	IO	64	
pciAD[10]	IO	63	
pciAD[11]	IO	62	
pciAD[12]	IO	61	
pciAD[13]	IO	60	
pciAD[14]	IO	59	
pciAD[15]	IO	57	
pciAD[16]	IO	44	
pciAD[17]	IO	43	
pciAD[18]	IO	41	
pciAD[19]	IO	40	
pciAD[20]	IO	39	
pciAD[21]	IO	37	
pciAD[22]	IO	36	
pciAD[23]	IO	35	
pciAD[24]	IO	32	
pciAD[25]	IO	31	
pciAD[26]	IO	29	
pciAD[27]	IO	28	
pciAD[28]	IO	27	
pciAD[29]	IO	26	
pciAD[30]	IO	25	
pciAD[31]	IO	24	
obTRG	O	103	Trigger pulse output
VCCIO	VCCIO	130	VCCIO, 3.3 or 5.0V
VCCIO	VCCIO	58	
VCC	VCC	19	VCC = 3.3V
VCC	VCC	7	
VCC	VCC	94	

Signal	Type	Pin	Description
VCC	VCC	114	
VCC	VCC	22	
VCC	VCC	42	
VCC	VCC	79	
VCC	VCC	91	
GND	GND	102	Power and Signal GND
GND	GND	122	
GND	GND	126	
GND	GND	138	
GND	GND	15	
GND	GND	30	
GND	GND	50	
GND	GND	54	
GND	GND	66	
GND	GND	87	
JTAG: TCK (Connect to GND)	I	109	JTAG
JTAG: TMS (Connect to VCC)	I	72	
STM(Connect to GND)	I	110	
JTAG: TDI (Connect to VCC)	I	38	
JTAG: TRSTB (Connect to GND)	I	71	
JTAG: TDO (Floating)	O	143	
NU (Connect to Gnd)	I	100	Unused inputs. Connect to GND.
NU (Connect to Gnd)	I	101	
NU (Connect to Gnd)	I	17	
NU (Connect to Gnd)	I	18	
NU (Connect to Gnd)	I	78	
NU (Connect to Gnd)	I	81	
NU (Connect to Gnd)	I	89	
NU (Connect to Gnd)	I	90	
NU (Connect to Gnd)	I	92	
NU (Connect to Gnd)	I	93	
NU (Do not connect)	O	144	Unused outputs. Do not connect.
NU (Do not connect)	O	5	
NU (Do not connect)	O	80	
NU (Do not connect)	O	82	
NU (Do not connect)	O	83	

Signal	Type	Pin	Description
NU (Do not connect)	O	84	
NU (Do not connect)	O	85	
NU (Do not connect)	O	86	
NU (Do not connect)	O	88	
NU (Do not connect)	O	95	
NU (Do not connect)	O	96	
NU (Do not connect)	O	97	
NU (Do not connect)	O	98	
NU (Do not connect)	O	99	

2.1 PCI Interface Notes

The interface of the iGPIB 72120 to the PCI bus is straightforward and does not require any additional components. Do identify the iGPIB 72120 on the PCI bus the following values are used.

Configuration space of the iGPIB 72120

Name	Value
Class	0x0780
Device ID	0x0011
Vendor ID	0x16da
Subsystem ID	0x0012
Subsystem Vendor ID	0x16da

2.2 GPIB Interface Notes

The iGPIB 72120 can be used with 3.3V or 5.0V PCI signal levels. The signal level used is defined by VCCIO pins of the circuit. The GPIB IEEE-488 specification specifies 5V TTL signal levels to be used on the GPIB lines. For that reason, the interface between the iGPIB 72120 and the GPIB is via general-purpose transceivers which provide the necessary voltage adaption.

Input Signal

To receive data from the GPIB, use SN74LVC244ADBDR buffers. Connect the A inputs of the buffer to the GPIB terminal and the Y output to the matching iGPIB 72120 input pin. Fix the buffers G input to low (i.e. always enabled). For the sixteen GPIB input lines, two SN74LVC244ADBDR are required.

Output Signals

To send data to the GPIB, use SN74LVTH125DBR buffers. Connect the data input of the buffer to the matching data output of the iGPIB 72120. Connect the output enable input of the buffer to the matching enable (oen) output of the iGPIB 72120. Connect the outputs of the buffer to the GPIB terminals by a 10 Ohms resistor each. For the sixteen GPIB output lines, four SN74LVTH125DBR are required.

Termination

The GPIB terminals require resistive termination to work according to the IEEE-488 specification. To provide the required termination, connect each GPIB signal line to VCC and GND by two resistors RL1 and RL2, respectively.

Resistive Termination Values

VCC	RL1(VCC)	RL2(GND)	Tolerance
5.0V	3.0 kOhms	6.2kOhms	5%
3.3V	1.8 kOhms	8.2kOhms	5%

3 Register Set

The iGPIB 72120 provides 17 registers (8 write/9 read). The lower 8 registers are compatible to the NEC 7210 registers.

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
D7	D6	D5	D4	D3	D2	D1	D0	0	R	Data In
B7	B6	B5	B4	B3	B2	B1	B0	0	W	Byte Out
CPT	APT	DET	END	DEC	ERR	DO	DI	1	R	Interrupt Status 1
CPT	APT	DET	END	DEC	ERR	DO	DI	1	W	Interrupt Mask 1
INT	0	LOK	REM	0	LOKC	REMC	ADSC	2	R	Interrupt Status 2
0	0	DMAO	DMAI	0	LOKC	REMC	ADSC	2	W	Interrupt Mask 2
S8	PEND	S6	S5	S4	S3	S2	S1	3	R	Serial Poll Status
S8	rsv	S6	S5	S4	S3	S2	S1	3	W	Serial Poll Mode
0	0	SPMS	LPAS	TPAS	LA	TA	MJMN	4	R	Address Status
ton	lon	0	0	0	0	ADM1	ADM0	4	W	Address Mode
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	5	R	Command Pass Through
CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	5	W	Auxiliary Registers
0	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	6	R	Address 0
ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	6	W	Address 0/1
EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	7	R	Address 1
EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	7	W	EOS
F1	F2	F3	CEN	CR3	CR2	CR1	CR0	0xE	R	Core Parameter Register

3.1 Data Registers

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
D7	D6	D5	D4	D3	D2	D1	D0	0	R	Data In
B7	B6	B5	B4	B3	B2	B1	B0	0	W	Byte Out

These data registers are used for transferring commands and data between the GPIB and the microcomputer system.

The Data In Register holds data sent from the talker over the GPIB when the iGPIB 72120 is addressed as the listener. Data is output over the data bus with a read operation. The contents of the Data In register is held until the next byte is received.

The Byte Out register holds data or a command written to it by a write operation and sends the data or command to the GPIB. The contents of the Byte Out register is updated by a write operation.

3.2 Interrupt Registers

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
CPT	APT	DET	END	DEC	ERR	DO	DI	1	R	Interrupt Status 1
CPT	APT	DET	END	DEC	ERR	DO	DI	1	W	Interrupt Mask 1
INT	0	LOK	REM	0	LOKC	REMC	ADSC	2	R	Interrupt Status 2
0	0	DMAO	DMAI	0	LOKC	REMC	ADSC	2	W	Interrupt Mask 2

The interrupt registers are composed of interrupt status bits, interrupt mask bits and other bits not associated with interrupts. Reading an interrupt state registers clears the corresponding interrupts. All interrupts can be masked by writing to the interrupt mask register at the corresponding address. Any bit set in the interrupt mask register causes an interrupt, if a 1 occurs in the corresponding interrupt status register.

3.2.1 Interrupt Bits in the Interrupt Status Registers

CPT	Command Pass Through. This bit indicates that an undefined command has been received via the GPIB or that a secondary command has been received following to an unknown command. It will only be set if the auxiliary register bit B0=1, which makes it possible to pass unknown commands (i.e. not decoded by the iGPIB 72120) to the processor. The handshake will be held off until the auxiliary command "valid" is issued by the CPU.
APT	Address Pass Through. This bit indicates that a secondary address has been received, which has to be checked by the CPU. This is only provided in address mode 3. The handshake will be held off until one of the auxiliary commands "valid" or "not valid" is issued by the CPU.
DET	Device Trigger. This bit indicates that a trigger message (GET when LADS) has been received.
END	END message received. This bit indicates that either the EOI or the EOS (Data In register equals EOS register) message has been received.
DEC	This bit indicates that a clear (DCL, or, SDC when LADS) message has been received.
ERR	Error. This bit indicates that the contents of the Byte Out register has been lost. It will be set if data has been sent without listener addressed or if a byte has been written to the Data Out register during source idle state (SIDS).
DO	Data Out. This bit indicates a data write request to the Byte Out register.
DI	Data In. This bit indicates a reception of a data byte from the GPIB Bus. In continuous mode it will never be set.
LOKC	Lockout Change. This bit indicates that the LOK-bit in interrupt status register 2 has changed.
REMC	Remote Change. This bit indicates that the REM-bit in interrupt status register 2 has changed.
ADSC	Address Status Change. This bit indicates that one of the bits TA, LA, CIC or MJMN has changed in the address status register.

3.2.2 Non Interrupt Bits in the Interrupt State Registers

LOK, REM	Lockout, Remote. These bits indicate the state of the RL (Remote/Local) functions. The LOK bit indicates that the function is in local(remote) with lockout state (LWLS or RWLS). The REM-bit indicates that the function is in remote state (REMS) or remote with lockout state (RWLS), respectively.
----------	--

DMAO, DMAI DMA Output, DMA Input. These bits control the DMA transfer between memory and the GPIB bus. If DMAO=1, and the Byte Out register is not full, a DMA request will be generated. If DMAI=1, a DMA request will be generated as soon as a byte has been received from the GPIB bus.

INT Interrupt. This bit indicates that an interrupt has occurred. It is generated by an OR operation of all unmasked interrupt bits.

3.3 Serial Poll Register

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
S8	PEND	S6	S5	S4	S3	S2	S1	3	R	Serial Poll Status
S8	rsv	S6	S5	S4	S3	S2	S1	3	W	Serial Poll Mode

The serial poll register can be read or written. The CPU writes the status byte (STB) into this register, which is sent when the GPIB system's Controller in Charge performs a serial poll. If the CPU sets the "rsv" bit to 1, the internal message *rsv* will be set. This generates a service request (SRQ line asserted) as soon as the chip is not in SPAS state. The *rsv* bit is cleared during serial poll (resets the SRQ line). The CPU can read the status byte (STB), written to the serial poll mode register, from the serial poll status register. Testing the PEND bit checks if the serial poll request has been serviced: the PEND bit is set when the rsv bit becomes 1. It is cleared when the serial poll function changes from APRS to NPRS. This way software can check if the the GPIB controller has already recognized the service request by a serial poll.

3.4 Address Mode and Status Registers

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
ton	lon	0	0	0	0	ADM1	ADM0	4	W	Address Mode

The Address Mode register is used to set the address mode. The states of various interface functions can be read from the Address Status register.

In the Address Mode register the bits ton, lon, ADM0 and ADM1 specify the address mode:

ton	lon	ADM1	ADM0	Address Mode	Addr. Reg. 0	Addr. Reg. 1
1	0	0	0	talk only	not used	not used
0	1	0	0	listen only	not used	not used
0	0	0	1	Address Mode 1	1st talker-(listener-) address	2nd talker-(listener-) address
0	0	1	0	Address Mode 2	primary talker-(listener-) address	secondary talker-(listener-) address
0	0	1	1	Address Mode 3	1st primary talker-(listener-) address	2nd primary talker-(listener-) address

Talk only or Listen only (ton or lon = 1)

In this modes, the recognition of the device address is not required. Therefore, the address registers are not used.

Address-Mode 1

In this mode, only primary addresses are used for talker and listener addressing. Up to two primary device addresses will be recognized.

Address-Mode 2

Talker/listener are operating in extended mode (TE, LE). Primary and secondary addresses are required to perform addressing. The recognition of primary and secondary address is managed by the hardware. A second primary address will not be recognized.

Address-Mode 3

Talker/listener are operating in extended mode (TE, LE). Primary and secondary addresses are required to perform addressing. The identification of the secondary address must be done by the CPU. Two primary device addresses may be recognized.

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
0	0	SPMS	LPAS	TPAS	LA	TA	MJMN	4	R	Address Status

The bits LPAS, TPAS, LA, TA, MJMN and SPMS indicate the states of the corresponding interface functions. LPAS and TPAS indicate the listener/talker primary addressed state. If enabled, changes of the bits LA, TA and MJMN initiate an ADSC interrupt. The bit SPMS (Serial Poll Mode State) indicates that a serial poll is in progress. It is set with SPE and it is cleared by SPD or IFC. MJMN is set on receipt of the 2nd talk or listen address. It is cleared on receipt of the 1st talk or listen address.

3.5 Address Registers

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	6	W	Address 0/1
-	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	6	R	Address 0
EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	7	R	Address 1

There are 2 address read registers and 1 address write register. Depending on the ARS-bit, the write register can access two 7-bit wide registers. Each of these registers contains a 5-bit wide address and the information whether this address represents a talker, a listener or both. The bit ARS (Address Register Select) specifies into which of the address registers the bits 0-6 shall be written (ARS=0 selects address register 0, ARS=1 selects address register 1). The specified address (AD1-AD5) will be recognized as talker address, if bit DT (Disable Talker) is 0. Bit DL (Disable Listener) = 0 specifies the address as a listener address. The bits DL0, DT0, DL1 and DT1 in the read registers correspond to the DL and DT bits in the corresponding write register. The bit EOI indicates the state of the EOI line at the time when the current data byte found in the data-in register has been received.

3.6 Command Pass Through Register

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	5	R	Command Pass Through

The CPT-register can be used to determine the state of the data lines of the GPIB. This is necessary if a DAC holdoff has been initiated and the CPU must qualify the current interface message.

3.7 EOS Register

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	7	W	EOS

The EOS register holds the seven- or eight-bit EOS message used by the GPIB interface to detect the end of a data block transfer. The width of EOS recognition is specified by the auxiliary register bit A4 (EOS-width).

3.8 Auxiliary Registers

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
0	0	0	C4	C3	C2	C1	C0	5	W	Auxiliary Command Execution
0	1	1	U	S	P2	P1	P0	5	W	Parallel Poll Register
1	0	0	A4	A3	A2	A1	A0	5	W	Auxiliary. Register A
1	0	1	B4	0	B2	B1	B0	5	W	Auxiliary. Register B
1	1	0	0	E3	E2	E1	E0	5	W	Auxiliary. Register E

The auxiliary register system consists of 4 auxiliary registers and 2 command registers. All these registers are accessed by a write operation to address 5. The data bit 7-5 select the target auxiliary register or command, respectively. Do not write to undefined auxiliary registers.

3.8.1 Auxiliary commands

Auxiliary commands are initiated by writing the byte 000C4C3C2C1C0 from the CPU into the auxiliary register. These commands are used to signal internal messages and to specify various operating modes.

Immediate Execute pon 00000

This command inverts the state of the internal message pon (POWER ON). If pon=1 all interface functions are placed in their idle states. Note: pon is 1 after Reset.

Chip Reset 00010

Chip Reset sets pon=1. All registers are cleared.

Finish Handshake 00011

This command finishes handshake by releasing the RFD holdoff state.

Trigger 00100

The command generates a trigger pulse at pin obTrig. obTrig is also pulsed in the active state of the Device Trigger function (DTAS), i.e. when a GET command is received from the Controller in Charge.

Return to Local 0X101

This command generates the internal message RTL. If X=1, then RTL will be set, otherwise RTL will be reset or pulsed, respectively.

Send EOI 00110

The next data byte written to the Byte Out register will be sent with the END message true. This can only be done in TACS.

Not Valid 00111

A handshake that has been held off by "address pass through" will continue. The secondary address is qualified as "not valid" by the CPU.

Valid 01111

A handshake that has been held off by "address pass through", will continue. The secondary address is qualified as "valid" by the CPU.

Set Parallel Poll Flag 0X001

This command sets the parallel poll flag to the value of bit C3(X). If the auxiliary register bit B4 is 0, the value of this flag is handled as internal message "ist" (individual status). Otherwise the service request state (SRQS) is used as "ist" signal.

Listen 10011

Listen pulses the internal message "ltn". If necessary, the continuous mode is disabled.

Listen in Continuous Mode 11011

This command pulses the internal message "ltn". In addition, the continuous mode will be enabled. This mode will be disabled when the auxiliary command "ltn" is detected or LIDS (listener idle state) is entered.

Local Unlisten 11100

This command pulses the internal message "lun".

3.8.2 Parallel Poll Register

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
0	1	1	U	S	P2	P1	P0	5	W	Parallel Poll Register

Writing the byte 011USP3P2P1 to the auxiliary register allows to write to the parallel poll register. When using the subset PP1 (remote configuration) it should not be written to this register. In this case the PPE message issued by the controller defines the parallel poll message. A PPD message issued by the controller disables the parallel poll response.

When using subset PP2 (local configuration) the response message must be written to this register in advance. The parallel poll response line is specified by the first 3 bits of this register. The 4th bit specifies if the chosen line will be set true or false on occurrence of the internal message "ist" (individual status): The message will be set true if "ist" equals bit S (4th bit). The 5th bit U contains the internal message "lpe~". If U = 0, the response to the parallel poll response is enabled. If U = 1, the parallel poll response is disabled and the bits S and P1-3 have no meaning, they should be reset to 0.

3.8.3 Auxiliary Register A

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
1	0	0	A4	A3	A2	A1	A0	5	W	Auxiliary Register A

The 5 bits of the auxiliary register A are used to specify handshake mode and the EOS message handling. The bits A0 and A1 specify the handshake mode. The bits A2, A3 and A4 specify the EOS handling:

A1	A0	Handshake Mode
0	0	normal
0	1	Blocked RFD message for all data
1	0	Blocked RFD message for END message
1	1	Continuous mode

Bit	Value	Function	
A2	1	Set	END interrupt bit set when EOS received
	0	Don't set	
A3	1	Send	EOI automatically on EOS sent
	0	Don't send	
A4	1	8-bit	width of EOS comparison
	0	7-bit	

3.8.4 Auxiliary Register B

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
1	0	1	B4	0	B2	B1	B0	5	W	Auxiliary Register B

The auxiliary register B specifies special hardware features of the interface.

Bit	Value	Function	
B0	1	Set	CPT interrupt bit set on the detection of an unknown GPIB command
	0	Don't set	
B1	1	Send	END with the status byte in SPAS
	0	Don't send	
B2	1	500ns	T1 speed for all data bytes transmitted except the first byte.
	0	standard	
B4	1	ist=SRQS	source of the ist local message.
	0	ist=Parallel Poll Flag	

Note

The B3 bit appearing in the original NEC 7210 has been removed from the design. The polarity of the INT pin always depends on the bus interface unit.

3.8.5 Auxiliary Register E

D7	D6	D5	D4	D3	D2	D1	D0	Adr. (HEX)	R/W	Name
1	1	0	0	0	0	E1	E0	5	W	Auxiliary Register E

The auxiliary register E consists of 2 bits. They specify the DAC holdoff handling.

Bit	Value	Function	
E0	1	Enables	DAC holdoff in DCAS (DCL, SDC command received)
	0	Disables	
E1	1	Enables	DAC holdoff in DTAS (GET command received)
	0	Disables	

4 Using the iGPIB 72120

4.1 Processing Undefined Commands

When $B0=1$, the DAC message is held false and the CPT bit is set when an undefined command is received. The CPU reads the undefined code via the CPT register. The handshake that stopped is completed when the Valix auxiliary command is issued.

When $B0=0$, the handshake is completed, just as when a defined command is received, and the CPT bit remains 0. The received code is ignored.

A secondary command received immediately after an undefined primary command is handled as an undefined command.

4.2 Processing Address Pass Through

The APT bit is set when the secondary address is received. This is the case when a secondary command is received in address mode 3 and $LPAS+TPAS=1$.

- In Address Mode 3 ($ton=lon=0$ and $ADM1=ADM0=1$) the TE and LE interface functions are used as the talker and listener, respectively. Address register 0 holds the first primary address and address register 1 holds the second primary address.
- The $LPAS+TPAS=1$ condition is satisfied when either the MTA (My Talk Address) or the MLA (My Listen Address) has been received.

When the APT bit is set, the handshake stops with the DAC messages held false just as when the CPT bit is set. The CPU must then perform the following:

- determine whether the secondary command just received is a listen, talk, major, or minor address by reading the LPAS, TPAS, and MJMN bits of the address status register
- determine whether the secondary command read through the CPT register is my address. If it is my address, the Valid auxiliary command must be issued. If it is not my address, the Non-valid auxiliary command must be issued.

When the Valid auxiliary command is received, the iGPIB 72120 assumes that the MSA (My Secondary Address) message has been received. When this command is issued, $LADS=TIDS:=1$ (if $LPAS=1$) or $TADS=LIDS:=1$ (if $TPAS=1$) is set, the DAC message is sent true, and the handshake is finished. When the Non-valid auxiliary command is received, the iGPIB 72120 assumes that the OSA (Other Secondary Address) message has been received. The core set $TIDS:=1$ (if $TPAS=1$) the DAC message is sent true, and the handshake is finished.

4.3 Transmitting Data

When a data request is received ($DO=1$), one byte of data is transmitted by a write to the Byte Out register. This process is repeated to send several bytes. The DO bit is cleared when the interrupt status register is read, or, when a write is made to the Byte Out register.

You can use DMA for sending or receiving data. When a request to send data is received and $DMAO=1$, or when new data can be written to the Byte Out register and $DMAI=1$, a DMA request is generated ($DMAREQ=1$).

Note

DMA might not be available on all bus interface units.

4.4 Receiving Data

When the CPU receives a data receive request, the contents of the Data In register is read. Data is received in the four modes below.

Normal Handshake Mode (A0=A1=0)

The device receives data as a listener, a data receive request (DI=1) is made and the RFD message is sent false. When the data is read from the Data In register, the RFD message is sent true, informing the talker that the listener is ready for the next data.

RFD Holdoff on All Data Mode (A0=1, A1=0)

When the device receives data as a listener, a data receive request (DI=1) is made and the RFD message is sent false, just as in normal handshake mode. However, even if the CPU reads the received data from the Data In register, the RFD message is held false until the Finish Handshake auxiliary command is issued. While the RFD message is being held false, the next data byte is not received and the contents of the Data In register is not updated. Therefore, the CPU can read the same data several times, if desired.

RFD Holdoff on End Mode(A0=0, A1=1)

In this mode, the RFD message is sent and held false when the data is received with the END bit set. Issue the Finish Handshake auxiliary command to send the RFD message true. The function is the same as in normal handshake mode unless the END bit is set.

Continuous Mode

In this mode, the RFD message is sent true in response to the DAV message unless the END bit is set. When the END bit is set, operation proceeds as in RFD Holdoff in End mode. This mode is used for data block end detection.

4.5 Completing Data Block Transfer

In accordance with IEEE Std. 488-1987, the following two methods are provided for detecting the end of a data block.

Placing EOS Byte After Data Block

The EOS code may be user-defined, but it is not possible to identify the EOS message if a code appearing in the data block is used. You may not use it if the data block contains arbitrary eight-bit data bytes. If ASCII code is used, use the LF code as EOS and the others as data bytes.

The transmission of the EOS byte works the same way as the transmission of a data byte. When DO=1, the EOS message can be transmitted by writing the EOS code to the Byte Out register.

Using the EOI Line

In this method, the END message (EOI=1) is sent out with the last byte of the data block.

In order to transmit the END message, use the Send EOI auxiliary command. After the Send EOI auxiliary command is issued to the iGPIB 72120 the END message is transmitted with the next data byte written to the Byte Out register.

When A3=1 (Output EOI on EOS Sent), the END message is sent when the EOS message is sent (based on the contents of the Byte Out register, the EOS register, and the value of A4).

Detecting the EOS Message

When A2=1 (End on EOS Received), the END bit is set when the EOS message is received. Receipt of the EOS message is controlled by the contents of the Data In register, the EOS register, and the value of A4.

Detecting the END Message

The END bit is set when the END message is received in LACS. You can identify the END or EOS message because the value of the EOI line is latched in the EOI bit when data is received and data itself is latched in the Data In register.

4.6 Serial Polling

To request service, you must confirm that there is no pending service request (PEND=0). Write the STB into the serial poll mode register with the local message rsv=1. If the device is not in SPAS, the SRQ message is sent true as soon as the rsv message is set. If the device is in SPAS, the SRQ message remains false until the serial polling is complete (SPAS=0). The PEND bit indicates whether a service request is accepted or left pending. It is set when rsv=1 and cleared then the STB is read out by the controller-in-charge (SPAS=0), or when the local message rsv is cleared before SPAS=1.

The STB set to the serial poll mode register is sent out when the STB is asked to send. The STB is sent only once even if the controller does not assert ATN after the first transfer. The END message is sent out with the STB if B1=1.

4.7 Parallel Poll Protocol

Before a parallel poll is executed, you must specify the which line of DIO1 to DIO8 the one bit status (ist:individual status) should be output and which polarity should be used. The following two methods are provided for this.

Remote Configuration (PP1)

In this method, the specifications are made by either PPE or PPD messages sent from the controller. Specifications by the CPU are not required in Remote Configuration.

Local Configuration (PP2)

In this method, the specifications are made locally at the device. In the Local Configuration you must write the appropriate bit values to the parallel poll register.

5 Timing Specifications

The PCI bus interface timing is in accordance to the PCI Specification 2.2. The GPIB bus timing is as specified in IEEE Std. 488.1-1987.

6 Electrical Specifications

Stresses beyond those listed in 'Absolute Maximum Ratings' may cause permanent damage to the circuit. The functional operation is made sure only within the limits of the 'Operating Range'. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V ... 4.6 V	DC Input Current	±20 mA
VCCIO Voltage	-0.5 V ... 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V ... VCCIO +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Operating Range

Symbol	Parameter	Mil. Min.	Mil. Max.	Ind. Min.	Ind. Max.	Com. Min.	Com. Max.	Unit
VCC	Supply Voltage	3.0	3.6	3.0	3.6	3.0	3.6	V
VCCIO	I/O Input Tolerance Voltage	4.75	5.5	4.75	5.5	4.75	5.25	V
TA	Ambient Temperature	-55	-	-40	85	0	70	°C
TC	Case Temperature	-	125	-	-	-	-	°C

AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
FC	Clock Frequency		30.0	33.3	MHz
TCH	Clock High Time		40% of nominal period	60% of nominal period	ns
TCL	Clock Low Time		40% of nominal period	60% of nominal period	ns

The PCI clock may not be stopped or slowed down in order to keep the GPIB interface core running. If the PCI clock is stopped or slowed down, the GPIB interface will cease to work with unpredictable results for the GPIB operation.

DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
VIH	Input HIGH Voltage		0.5 VCC	VCCIO+0.5	V
VIL	Input LOW Voltage		-0.5	0.3 VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4	VCC	V
		IOH = -500 µA	0.9 VCC	VCC	V
VOL	Output LOW Voltage	IOL = 16 mA(a)		0.45	V
		IOL = 1.5 mA		0.1 VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	µA



Symbol	Parameter	Conditions	Min.	Max.	Units
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	μ A
CI			10	pF	
IOS	Output Short Circuit Current(c)	VO = GND	-15	-180	mA
		VO = VCC	40	210	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	μ A

Power-Up Sequencing

When powering up a device, the VCC/VCCIO rails must take 400 μ s or longer to reach the maximum value.

NOTE: Ramping VCC/VCCIO to the maximum voltage faster than 400 μ s can cause the device to behave improperly.

7 Mechanical and Chemical Specifications

7.1 RoHS Conformance

Meeting the RoHS Directive (2002/95/EC) the iGPIB 72120 is lead free (Pb-free). INES has chosen the Sn/Ag/Cu alloy as the solder ball alloy for laminate/ball grid array products, and Sn(matte) as the lead finish for lead-frame based products.